What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. An analog to digital converter comprising:

an input stage having an input and including a sample and hold circuit;

a plurality of analog to digital stages serially coupled with said input stage and with one another; and

a reference voltage circuit adapted to provide a reference voltage to each analog to digital stage of said plurality of analog to digital stages, the reference voltage circuit comprising:

a programmable current supply coupled in series with a resistor and an active load between a source of supply potential and a source of ground potential;

a differential amplifier having a first differential input and a second differential input, said first differential input coupled through a first capacitor and a switching device to a first terminal of said resistor, said second differential input coupled through a second capacitor and a second switching device to a second terminal of said resistor;

a third switching device having a first end coupled to said first capacitor and to said first switching device, and a second end coupled to said second capacitor and to said second switching device;

a third capacitor coupled between a first differential output of said differential amplifier and said first differential input;

a fourth capacitor coupled between a second differential output of said differential amplifier and said second differential input;

a fourth switching device coupled in parallel with said third capacitor and adapted to switchingly bypass said third capacitor; and

a fifth switching device coupled in parallel with said fourth capacitor and adapted to switchingly bypass said fourth capacitor.

2. A switched capacitor voltage source comprising:

a reference voltage supply including a programmable current source coupled in series with a standard resistor and an active load device, said reference supply having a first two terminal output disposed across said resistor;

a sampling circuit including a first capacitor, a second capacitor, and a switching device, said sampling circuit including a second two terminal input coupled to said first two terminal output and a third two terminal output; and

a precision differential amplifier including a fourth two terminal input, a fifth two terminal output, and first and second feedback paths coupling said fifth two terminal output to said fourth two terminal input, said fifth two terminal output adapted to output a first voltage related to a second voltage impressed on said resistor by said program current source.

3. A switched capacitor voltage source as defined in claim 2 wherein an output impedance measured at said fifth two terminal output is substantially lower than an impedance of said resistor.

4. A switched capacitor voltage source as defined in claim 2 wherein said first and second feedback paths are adapted to produce unity gain between said fourth two terminal input and said fifth two terminal output, and wherein said first voltage is related to said second voltage by a factor substantially equal to one.

5. A switched capacitor voltage source as defined in claim 2 wherein said first and second feedback paths each includes a respective capacitor and a respective switching device, said respective switching device being adapted to switchingly shunt said respective capacitor.

6. A reference voltage source circuit for an analog to digital converter comprising:

a programmable current source having a first control input and a current output;

a reference impedance device having first and second ends, said first end coupled to said current output and said second end coupled through a load to a source of constant potential;

a sample and hold circuit having first and second sample and hold inputs coupled to said first and second ends of said reference impedance device respectively, said sample and hold circuit having first and second sample and hold outputs;

a differential amplifier circuit having first and second differential amplifier inputs respectively coupled to said first and second sample and hold outputs, said differential amplifier circuit having first and second differential amplifier outputs, said differential amplifier circuit including respective feedback paths between said differential amplifier outputs and differential amplifier inputs; and

a feedback circuit including first and second feedback inputs respectively coupled to said first and second differential amplifier outputs, said feedback circuit including a second control input and a control output, said control output being coupled to said first control input of said programmable current source.

7. A reference voltage source circuit for an analog to digital converter as defined in claim 6 wherein said first control input comprises:

a digital control input.

8. A reference voltage source circuit for an analog to digital converter as defined in claim 6 wherein said reference impedance device comprises:

a variable resistor.

9. A voltage source adapted for use in an analog to digital converter comprising:

a switched capacitor circuit including a sample and hold portion and an amplifier portion, said sample and hold portion having an output coupled to an input of said amplifier portion, said sample and hold portion including a switching device for sampling an input voltage and a capacitive device for holding the input voltage, said amplifier portion including a differential amplifier having first and second feedback paths respectively coupled

from a first output to a first input and from a second output to a second input of said differential amplifier.

10. A voltage source as defined in claim 9 further comprising a digital to analog converter having output coupled to said sample and hold portion for providing said input voltage to said sample and hold portion.

11. A voltage source as defined in claim 10, wherein said digital to analog converter comprises:

an adjustable current source;

an active load transistor; and

a reference resistor having a first terminal coupled to said adjustable current source and a second terminal coupled to said active load transistor, said reference resistor adapted to provide said input voltage between said first and second terminals in response to an output current produced by said adjustable current source.

12. A sampled voltage source comprising:

a reference resistor adapted to receive a programmed current to produce a programmed voltage;

a sampling circuit including first and second capacitors with respective first and second switches and a crowbar switch, an input of said sampling circuit coupled across said reference resistor to sample said programmed voltage; and

a differential amplifier having output impedance substantially lower than an impedance of said reference resistor, said differential amplifier having an input coupled across an output of said sampling circuit, said differential amplifier including a feedback circuit coupled between said output of said amplifier and said input of said amplifier.

13. A programmable voltage supply comprising:

a digital input adapted to receive a numerical value corresponding to a desired output voltage;

a first output adapted to output an analog voltage corresponding to said digital input;

a voltage generator having a second output with a first impedance, said voltage generator coupled to said digital input and adapted to translate said numerical value into a first voltage;

a sampling circuit switchingly coupled to said relatively high impedance output and adapted to receive and store said first voltage during a first time interval and to output said first voltage during a second time interval; and

amplifying means coupled to said sampling circuit for receiving said first voltage during said second time interval and for outputting a voltage on a third output said third output having a second impedance, said second impedance lower than said first impedance, said third output being coupled to said first output.

14. A circuit for producing a stable reference voltage comprising:

means for producing a first voltage across a resistor;

means for storing said first voltage as a second stored voltage; and

outputting means for outputting said second voltage as a third output voltage, said outputting means including a relatively high impedance input port and a relatively low impedance output port, said outputting means including negative feedback means.

15. A fully differential voltage supply comprising:

a first input line coupled between a first voltage source of a first potential and a first input of a differential amplifier, said first input line including a first sampling capacitor and a first sampling switch; and

a second input line coupled between a second voltage source of a second potential and a second input of said differential amplifier, said second input line including a second sampling capacitor and a second sampling switch, said first and second voltage sources mutually coupled by a resistor, said first and second sources switchingly coupled by a crowbar switch to provide signals on said respective input lines to the respective first and second inputs of said differential amplifier, said differential amplifier including a first output coupled to said first input and a second output coupled to said second input.

16. An imaging device comprising:

an array of pixels each providing a respective analog pixel output signal; and

an analog to digital converter for converting said analog pixel output signals to digital pixel output signals, said analog to digital converter comprising:

a conversion circuit having an analog signal input, first, second, third, and fourth reference signal inputs, and a digital signal output; and

a reference voltage circuit having a power supply input, a digital voltage setting input, and first, second, third, and fourth reference signal outputs respectively coupled to said first, second, third, and fourth reference signal inputs, said reference voltage circuit including a reference resistor coupled through a sample and hold circuit to fifth and sixth differential inputs of a fully differential amplifier with seventh and eighth differential outputs alternately switchingly coupled to said first, second, third, and fourth reference signal outputs.

17. An imaging device as defined in claim 16 wherein said fully differential amplifier includes first and second feedback circuits coupled between said sixth differential output and fifth differential input, and eighth differential output and seventh differential input respectively.

18. An imaging device as defined in claim 16 wherein said sample and hold circuit includes first and second transistors each coupled in series with a respective switching device between a respective end of said resistor and a respective one of said fifth and sixth differential inputs.

19. An imaging device as defined in claim 17 wherein said first and second feedback circuits each comprises:

a capacitor coupled in parallel with a switching device, said switching device adapted to switchingly shunt said capacitor.

20. An imaging device as defined in claim 16 further comprising:

respective first and second switching devices respectively switchingly coupled between said first reference signal output and said first reference signal input and between said second reference signal output and said second reference signal input.

21. An imaging device as defined in claim 16 further comprising:

respective first and second voltage dividing devices respectively switchingly coupled between said third reference signal output and said third reference signal input and between said fourth reference signal output and said fourth reference signal input.

22. A method of operating an imaging device comprising:

receiving an analog pixel output from an analog pixel at an analog pixel input of an analog to digital converter;

receiving first, second, third, and fourth reference signals at respective reference signal inputs of said analog to digital converter; and

generating said first, second, third, and fourth reference signals by:

receiving a numerical input at a numerically controlled current source;

receiving a reference current from said numerically controlled current source at an active load through a reference resistor;

receiving a reference voltage from across said reference resistor at a differential input of a sample and hold circuit to form a stored voltage;

receiving said stored voltage at a differential input of a differential amplifier;

receiving a feedback signal at said differential input of said differential amplifier from a differential output of said differential amplifier to produce said first and second reference signals; and

receiving said first and second reference signals at a differential input of a voltage divider circuit to produce said third and fourth reference signals.

23. Method of operating an imaging device as defined in claim 22 wherein said producing said voltage divider circuit comprises a capacitive voltage divider circuit.

24. A method of producing first and second reference voltages for a pipeline analog to digital converter comprising:

flowing a substantially constant current through a resistor coupled in series with a transistor, said transistor configured as an active load;

sampling a first voltage from a first node at first end of said resistor onto a first plate of a first capacitor through a first switching device during a first time interval;

sampling a second voltage from a second node at a second end of said resistor onto a second plate of a second capacitor through a second switching device during said first time interval;

holding third and fourth plates of said first and second capacitors respectively at a common voltage during said first time interval by switchingly coupling said third and fourth plates to a source of said common voltage through respective third and fourth switching devices;

switchingly decoupling said third and fourth plates from said common voltage during a second time interval;

switchingly decoupling said first plate of said first capacitor from said first node during said second time interval;

switchingly decoupling said second plate of said second capacitor from said second node during said second time interval;

receiving a third voltage from said third capacitor plate at a first input of a differential amplifier;

receiving a fourth voltage from said fourth capacitor plate at a second input of said differential amplifier, said differential amplifier including negative feedback from a first output to said first input and from a second output to said second input; and

receiving a fifth voltage from said first output and a sixth voltage from said second output at an analog to digital conversion circuit.

25. A method as defined in claim 24 wherein said first and second and third and fourth and fifth switching devices each comprises a transistor.

26. A method as defined in claim 24 wherein flowing a substantially constant current through a resistor comprises:

applying a digital numerical input value to a digital input of a numerically controlled current supply, and outputting a current related to said numerical input value from an analog output of said numerically controlled current supply.

27. A method as defined in claim 24 wherein said act of including negative feedback from a first output to said first input and from a second output to said second input comprises:

coupling a third capacitor between said first output and said first input;

coupling a fourth capacitor between said second output and said second input;

switchingly activating said third capacitor by opening a sixth switching device coupled in parallel therewith; and

switchingly activating said fourth capacitor by opening a seventh switching device coupled in parallel therewith.

28. A method of converting an analog input signal to a digital output signal comprising:

sampling a differential reference voltage onto a first plate of a first sampling capacitor with reference to a second plate of a second sampling capacitor during a first time interval, said first and second sampling capacitors including respective third and fourth plates, said the third and fourth plates having a common electrical potential during the first time interval;

switchingly electrically coupling said first and second plates of said first and second sampling capacitors respectively whereby electrical charge is transferred between said first and second plates;

applying a resulting differential voltage on said third and fourth plates to a positive input and a negative input respectively of a differential amplifier during a second time interval, said differential amplifier having a positive output and a negative output;

electrically coupling an output voltage at said positive output to said positive input through a first feedback capacitor during said second time interval; and

electric coupling an output voltage at said negative output to said negative input through a second feedback capacitor during the second time interval.

29. A method of converting an analog input signal to a digital output signal as defined in claim 28 comprising:

switchingly electrically coupling said third and fourth plates of said first and second sampling capacitors to a source of a reference potential during said first time interval.

30. A method of converting an analog input signal to a digital output signal as defined in claim 28 wherein said first and second and third and fourth capacitors have equal capacitance.

31. A method of converting an analog input signal to a digital output signal as defined in claim 28 comprising maintaining a differential output voltage between said positive and negative outputs of said differential amplifier during said second time, said differential output voltage equal to said differential reference voltage.

32. A method of operating a pipeline analog to digital converter comprising:

applying a digital input through a digital to analog converter to produce a standard current;

receiving said reference current through a standard resistor to generate a standard voltage;

receiving said standard voltage across respective first and second differential inputs of a capacitive crowbar circuit during a first time interval;

closing a crowbar switch of said capacitive crowbar circuit to produce a crowbar circuit output voltage;

receiving said crowbar circuit output voltage across respective third and fourth differential inputs of a differential amplifier to produce a differential reference voltage across

respective first and sixth differential outputs of said differential amplifier, said differential amplifier including a negative feedback circuit;

receiving said differential reference voltage at a capacitive divider circuit to produce first and second divided reference voltages at respective first and second differential outputs of said capacitive divider circuit during a third time interval; and

receiving said differential reference voltage at said divided reference voltages at respective inputs of an ADC stage of a pipeline ADC during a fourth time interval.

33. A method of operating a pipeline analog to digital converter as defined in claim 32 wherein the differential amplifier and negative feedback circuit exhibits unity gain.

34. An integrated circuit comprising:

a processing unit;

an analog to digital converter;

a digital signal path for coupling said processing unit to said analog to digital converter;

a fully differential reference voltage supply coupled to said analog to digital converter by means of a differential signal path, said fully differential reference voltage supply comprising:

a reference resistor adapted to exhibit a reference voltage between first and second nodes thereof in response to a reference current impressed thereupon;

a fully differential amplifier circuit having third and fourth differential signal input nodes, a common mode voltage input node, and fifth and sixth differential signal output nodes, said third and fourth differential signal input nodes coupled to said first and second nodes respectively through respective first and second capacitors, said fifth and sixth differential signal output nodes coupled to said third and fourth differential signal input nodes respectively through respective third and fourth capacitors;

a source of common mode voltage adapted to be switchingly coupled to both said third and fourth differential signal input nodes;

first and second switching devices adapted to switchingly shunt said third and fourth capacitors respectively; and

a third switching device adapted to switchingly couple said first and second nodes.

35. A CMOS image sensor comprising:

a first plurality of pixel cells disposed in an array configuration on a semiconductor substrate, said array configuration including a plurality of rows of said cells and a plurality of columns of said cells;

a plurality of row lines respectively coupled to said plurality of rows of said cells;

a plurality of column lines respectively coupled to said plurality of columns of said cells;

a row decoder coupled to said plurality of row lines and adapted to impress a plurality of electrical signals thereon; and

an analog to digital converter switchingly coupled to said plurality of row lines and adapted to receive a plurality of electrical signals from said plurality of columns of said cells respectively coupled thereto, said analog to digital converter including a voltage reference source having:

a switched capacitor circuit including a sample and hold portion and an amplifier portion, said sample and hold portion including a switching device for differentially sampling an input voltage across a resistor and a capacitive device for holding said input voltage, said amplifier portion including a differential amplifier having first and second feedback paths respectively coupled from a first output to a first input and from a second output to a second input of said differential amplifier.

36. An electronic circuit comprising:

an analog signal source coupled to an analog input of an analog to digital converter; and

a reference voltage supply circuit having a differential output coupled to a differential input of said analog to digital converter, said reference voltage supply including:

a current source adapted to produce a reference current;

a resistor coupled to said current source and adapted to convert said reference current into a precision voltage;

a sampling circuit including a first capacitor, a second capacitor, and a crowbar switch, said sampling circuit having a first differential input coupled to respective first sides of said first and second capacitors, said sampling circuit having a second differential output coupled to respective second sides of said first and second capacitors; and

a precision differential amplifier having a third differential input coupled to said second differential output, said precision amplifier having a fourth differential output coupled to a differential input of said analog to digital converter whereby said analog to digital converter receives a low impedance signal corresponding to said precision voltage.

37. A method of controlling a programmable voltage supply comprising:

applying a digital value to a digital input of a programmable current source so that said programmable current source produces a first reference current;

receiving said first reference current through a resistor so that a second reference voltage exists across said resistor;

receiving said second reference voltage across an input of a capacitive network and storing said second reference voltage within said capacitive network;

switching said capacitive network so that a third transferred voltage exists across an output of said capacitive network; and

receiving said third transferred voltage at an input of a differential amplifier and processing said third transferred so that a fourth output voltage exists across an output of said differential amplifier.

38. A method of controlling a programmable voltage supply as defined in claim 37 further comprising:

configuring said differential amplifier as a unity gain amplifier.

39. A method of reducing amplifier offset in a reference voltage supply circuit for an analog to digital converter comprising:

receiving a first current through a reference resistor, said first current producing a reference voltage across said reference resistor;

receiving said reference voltage at an input of a sample and hold circuit and storing a stored voltage within said sample and hold circuit;

receiving said stored voltage from an output of said sample and hold circuit at an input of a differential amplifier;

receiving an amplifier output voltage from an output of said differential amplifier at an input of an analog digital converter;

producing said first current with a programmable current supply, said programmable current supply receiving a control signal controlling said first current; and

modifying said control signal to reduce an offset of said differential amplifier.

40. A method of reducing amplifier offset of in a reference voltage supply circuit for an analog to digital converter as defined in claim 39 wherein modifying said control signal to reduce an offset of said differential amplifier comprises:

receiving a null input at said input of said differential amplifier during a calibration time interval;

receiving said offset as an offset voltage signal from said output of said differential amplifier at an input of a feedback circuit during said calibration time interval;

receiving a current setpoint signal at a current setpoint input of said feedback circuit; and

outputting said control signal controlling said first current from an output of said feedback circuit, said control signal reflecting said current setpoint signal and said offset voltage signal.